REMARKS

This response amends Claims 1, 14 and 16 to ensure allowance of Claims 1-19. Now pending in the application are Claims 1-19, of which Claims 1, 14 and 16 are independent. Support for the amendments appear in the specification on page 6, line 14-16; page 7, line 26; Figure 6 and 11; and throughout the specification. The amendments present no new matter and they present no new issues. Thus, consideration of the proposed amendments requires no further search.

Claim Rejections - 35 U.S.C. §102

Claims 1-19 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,631,452 of Lin (hereinafter "Lin"). Applicants respectfully traverse each of these rejections for reasons discussed below. For ease of the discussion below, each respective related claim set is discussed separately.

Rejection of Claims 1-13 under 35 U.S.C. §102:

Claims 1-13 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Lin. Applicants respectfully traverse this rejection in view of the above amendments and the following arguments.

Amended independent Claim 1 recites a microprocessor that includes a detector for detecting an imminent register window overflow or underflow condition. The microprocessor also includes an instruction generator responsive to the detector for generating at least one instruction to manipulate the storage to avoid a trap to avoid stalling the microprocessor. The trap performs at least one of a register window spill operation or a register window fill operation responsive to the condition that is detected as imminent.

Applicants respectfully submit that Lin fails to disclose each and every element of amended Claim 1. More specifically, Applicants submit that Lin fails to disclose that the microprocessor avoids a trap performing at least one of the register window spill operation or a register window fill operation to avoid stalling the microprocessor.

Claims 2-13 depend directly or indirectly upon amended Claim 1, and therefore, incorporate the patentable features of amended Claim 1.

Lin discloses mandatory and speculative spill/fill operations. In Figure 6 of the Lin reference, the mandatory spill/fill operation (MOP) is performed when RSE related instructions (RI) are monitored and registers are not available in the register stack. *See*, Lin, column 8, lines 58-65. More specifically and in the words of the Lin, the speculative spill/fill operations are opportunistic spill/fill operations performed when RI is not monitored and bandwidth (BW) is available. In other words, absent sufficient bus bandwidth, Lin performs mandatory spill/fill operations. In the mandatory spill/fill operation, the processor is stalled until the mandatory spill/fill operation is completed. *See*, Lin, column 3, lines 2-5.

Lin, however, does not disclose that the processor includes a detector for detecting a register overflow or underflow condition is imminent and includes an instruction generator responsive to the detector to avoid a trap to avoid stalling the microprocessor. The trap performs at least one of a register spill operation or a register window fill operation responsive to the condition that is detected as imminent. In the Lin reference, performance of the speculative spill/fill operations is opportunistic. That is, in speculative spill/fill mode Lin does not detect a register overflow/underflow condition is *imminent*. Rather, in this mode Lin performs the spill/fill operation if sufficient bus bandwidth is available and upon detection of RI instructions. In the speculative spill/fill mode Lin stalls the processor and performs the spill/fill operation. Further, Lin discloses that even in the speculative spill/fill mode the register stack engine (RSE) will stall the processor and implement mandatory spill/fill operations, when a register overflow condition is *imminent*. *See*, column 8, lines 62-65 of Lin. Hence, Lin does not avoid a trap performing a spill/fill operation to avoid stalling the microprocessor when either a register overflow or underflow is *imminent*. Hence, Lin does not anticipate amended Claim 1.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 1-13 under 35 U.S.C. §102(e).

Rejection of Claims 14-15 under 35 U.S.C. §102:

Claims 14 and 15 stand rejected under 35 U.S.C. §102(e) as being anticipated by Lin. Applicants respectfully traverse this rejection in view of the above amendments and the following arguments.

Amended independent Claim 14 recites a microprocessor that includes a detector for detecting an instruction in a cache prior to execution of the instruction that indicates a trap requiring an access to storage to manage register window information is imminent.

Applicants respectfully submit that Lin fails to disclose each and every element of the claimed invention. More specifically, Applicants submit that Lin fails to disclose a microprocessor that includes a detector for detecting an instruction in a cache prior to execution of the instruction that indicates a trap requiring an access to storage to manage register window information is imminent and an instruction generator responsive to the detector for generating at least one instruction to avoid the trap. The trap performing at least one of a register window spill operation or a register window fill operation.

Claim 15 depends from amended independent Claim 14, and therefore, incorporates the patentable features of amended Claim 14.

Lin discloses mandatory and speculative spill/fill operations. In Figure 6 of the Lin reference, the mandatory spill/fill operation (MOP) is performed when RSE related instructions (RI) are monitored and registers are not available in the register stack. *See*, Lin, column 8, lines 58-65. The speculative, or in the words of Lin, opportunistic spill/fill operation is performed when RI is not monitored and bandwidth (BW) is available. In the mandatory spill/fill operation, the processor is stalled until the mandatory spill/fill operation is completed. *See*, Lin, column 3, line 2-5. Lin discloses that the mandatory spill/fill operations are not avoided but merely reduced by the opportunistic spill/fill operations.

Lin, however, does not disclose that the processor avoids the trap performing at least one of the register windows spill operation or a register window fill operation because a detector detects an instruction in a cache prior to execution of the instruction indicating that a trap requiring an access to the storage to manage register window information is imminent. Lin avoids a mandatory spill/fill operation if bus bandwidth is available without regard for what instructions are in cache.

In Lin, the need for the mandatory spill/fill operation is reduced by performing the speculative spill/fill operation. Although the need for the mandatory spill/fill operation is reduced as taught by Lin, the mandatory spill/fill is still required if RSE related instructions (RI) are monitored and registers are not available in the register stack. Lin does not avoid the mandatory spill/fill operation.

In the Office Action, it is noted that Lin teaches instructions are stored in an instruction cache they are then fetched from the instruction cache to be decoded and eventually executed. However, in contrast to Claim 14, Lin monitors instructions to carry out a mandatory spill/fill operation. That is, the microprocessor of Claim 14 monitors instructions in a cache to avoid a spill/fill operation such as a trap performing at least one of a register window spill operation or a register window fill operation. For at least these reasons, Applicants contend Lin does not anticipate amended Claim 14.

Accordingly, Applicants request the Examiner to reconsider and withdraw the rejection of Claim 14 under 35 U.S.C. §102(e).

Rejection of Claims 16-19 under 35 U.S.C. §102:

Claims 16-19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Lin. Applicants respectfully traverse this rejection in view of the above amendments and the following arguments. Amended independent Claim 16 recites a method performed in a microprocessor having a plurality of registers logically partitioned into register windows and a storage for storing contents of register windows. Performance of the method in the microprocessor determines that one of a register window overflow condition and a register window underflow condition is imminent by performing a logic operation on a value representative of a state of a register and a value representative of an instruction held in cache.

Applicants respectfully submit that Lin fails to disclose each and every element recited in amended Claim 16.

Claims 17-19 depend directly or indirectly upon amended independent Claim 16, and therefore, incorporate the patentable features of amended Claim 16.

As discussed above in relation to the rejections of Claims 1-15, Lin discloses mandatory and speculative, or opportunistic spill/fill operations. Lin monitors instructions to identify the mandatory spill/fill operations and performs the opportunistic spill/fill operations when certain attributes are set that allow such an operation and the bandwidth of a memory bus supports such an operation. However, Lin does not perform a logic operation on a value representative of a state of a register and a value representative of an instruction held in cache to determine that one of a register window overflow condition and a register window underflow condition is imminent. Amended Claim 16 includes the step of determining that one of a register window overflow condition and a register window underflow condition is

imminent by performing a logic operation on a value representative of a state of a register and a value representative of an instruction held in cache. Nowhere does Lin disclose such a step. For at least these reasons, Lin fails to anticipate Claims 16-19.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 16-19 under 35 U.S.C. § 102(e).

CONCLUSION

In view of the remarks set forth above, applicants contend that claims 1-19, presently pending in the application, are patentable and in condition for allowance. If the Examiner deems that there are any remaining issues, we invite the Examiner to call the undersigned at 617-227-7400.

Respectfully submitted,
LAHIVE & COCKFIELD, LLP

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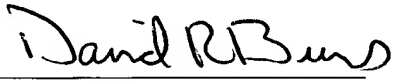
By 

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